

STRUCTURE AND METHOD FOR SCHEDULER PIPELINE DESIGN FOR HIERARCHICAL LINK SHARING

ABSTRACT OF THE DISCLOSURE

5 A pipeline configuration is described for use in network traffic management for
the hardware scheduling of events arranged in a hierarchical linkage. The configuration
reduces costs by minimizing the use of external SRAM memory devices. This results in
some external memory devices being shared by different types of control blocks, such as
flow queue control blocks, frame control blocks and hierarchy control blocks. Both
10 SRAM and DRAM memory devices are used, depending on the content of the control
block (Read-Modify-Write or 'read' only) at enqueue and dequeue, or Read-Modify-
Write solely at dequeue. The scheduler utilizes time-based calendars and weighted fair
queueing calendars in the egress calendar design. Control blocks that are accessed
infrequently are stored in DRAM memory while those accessed frequently are stored in
15 SRAM.